Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.An embedded memory chip, comprising:

a logic circuit;

a memory unit coupled to said logic circuit, wherein said logic circuit and said memory unit are fabricated substantially in a center area of said embedded memory chip;

a plurality of bonding pads situated on a peripheral area adjacent to said center area of said embedded memory chip; and

a built-in self test (BIST) circuit situated under at least one of said bonding pads for detecting faults in said embedded memory chip.

[c2] 2.The embedded memory chip according to claim 1 wherein a V_{DD} power is provided to said BIST circuit by said logic circuit through a V_{DD} power supply line that is situated under said bonding pads and encircles said center area.

[c3] 3.The embedded memory chip according to claim 2 wherein said logic circuit is coupled to a first switching device for controlling said V_{DD} power to said BIST circuit.

[c4] 4.The embedded memory chip according to claim 3 wherein said first switching device is a MOS transistor, and wherein said MOS transistor has a control gate that is electrically connected to said logic circuit, a source terminal that is biased to an external V_{DD} power supply node, and a drain terminal that is electrically connected to said V_{DD} power supply line.

[c5] 5.The embedded memory chip according to claim 3 wherein said first switching device is a PMOS transistor.

[c6] 6.The embedded memory chip according to claim 3 wherein said first switching device is not situated under any of said bonding pads.

[c7] 7.The embedded memory chip according to claim 1 wherein a V_{SS} power is provided to said BIST circuit by said logic circuit through a V_{SS} power supply line that is also situated under said bonding pads and encircles said center area.

[c8] 8.The embedded memory chip according to claim 7 wherein said logic circuit is coupled to a second switching device for controlling said V_{SS} power to said BIST circuit.

[c9] 9.The embedded memory chip according to claim 7

wherein said second switching device is an NMOS transistor.

[c10] 10.The embedded memory chip according to claim 7 wherein said second switching device is not situated under any of said bonding pads.

[c11] 11.An embedded memory chip, comprising:
a logic circuit;
a memory unit coupled to said logic circuit, wherein said logic circuit and said memory unit are fabricated substantially in a center area of said embedded memory chip;
a plurality of bonding pads situated on a peripheral area adjacent to said center area of said embedded memory chip; and
a built-in self test (BIST) circuit situated under at least one of said bonding pads, wherein said BIST circuit is activated when implementing an IC testing on said embedded memory chip for detecting faults in said memory unit and is deactivated as a disuse part of said embedded memory chip after finishing said IC testing.

[c12] 12.The embedded memory chip according to claim 11 wherein a V_{DD} power is provided to said BIST circuit by said logic circuit through a V_{DD} power supply line that is situated under said bonding pads and encircles said cen-

ter area.

[c13] 13.The embedded memory chip according to claim 12 wherein said logic circuit is coupled to a first switching device for controlling said V_{DD} power to said BIST circuit.

[c14] 14.The embedded memory chip according to claim 13 wherein said first switching device is a MOS transistor, and wherein said MOS transistor has a control gate that is electrically connected to said logic circuit, a source terminal that is biased to an external V_{DD} power supply node, and a drain terminal that is electrically connected to said V_{DD} power supply line.

[c15] 15.The embedded memory chip according to claim 13 wherein said first switching device is a PMOS transistor.

[c16] 16.The embedded memory chip according to claim 13 wherein said first switching device is not situated under any of said bonding pads.

[c17] 17.The embedded memory chip according to claim 11 wherein a V_{SS} power is provided to said BIST circuit by said logic circuit through a V_{SS} power supply line that is also situated under said bonding pads and encircles said center area.

[c18] 18.The embedded memory chip according to claim 17

wherein said logic circuit is coupled to a second switching device for controlling said V_{SS} power to said BIST circuit.

[c19] 19.The embedded memory chip according to claim 17 wherein said second switching device is an NMOS transistor.

[c20] 20.The embedded memory chip according to claim 17 wherein said second switching device is not situated under any of said bonding pads.